VT1720

PCI Multi-Channel Audio Controller

Revision 1.0
April 14, 2004

VIA Technologies, Inc.

Copyright Notice:

Trademark Notices:

VT1712, VT1724 and VT1720 may only be used to identify products of VIA Technologies.

Windows XP™. Windows 2000™. Windows ME™, Windows 98™, Windows 95™ and Plug and Play™ are registered trademarks of Microsoft Corp.
PCI™ is a registered trademark of the PCI Special Interest Group.
All trademarks are the properties of their respective owners.

Disclaimer Notice:

No license is granted, implied or otherwise, under any patent or patent rights of VIA Technologies. VIA Technologies makes no warranties, implied or otherwise, in regard to this document and to the products described in this document. The information provided by this document is believed to be accurate and reliable to the publication date of this document. However, VIA Technologies assumes no responsibility for any errors in this document. Furthermore, VIA Technologies assumes no responsibility for the use or misuse of the information in this document and for any patent infringements that may arise from the use of this document. The information and product specifications within this document are subject to change at any time, without notice and without obligation to notify any person of such change.

Offices:

USA Office:
940 Mission Court
Fremont, CA 94539
USA
Tel: (510) 683-3300
Fax: (510) 683-3301 or (510) 687-4654
Web: http://www.viatech.com

Taipei Office:
8th Floor, No. 533
Chung-Cheng Road, Hsin-Tien
Taipei, Taiwan ROC
Tel: (886-2) 2218-5452
Fax: (886-2) 2218-5453
Web: http://www.via.com.tw

Ordering Information:

VT1720 - 128PQFP

Revision History

Document Release	Date	Revision	Initials
1.0	4/14/04	Inital external release	EY

Table of Contents

List of Figures

List of Tables

VT1720
Envy24PT
PCI Multi-Channel Audio Controller

Product Features

- PCI 2.2 interface with bus mastering and burst modes
- 24-bit resolution audio format support
- Bit accurate transfers
- Sampling rates up to 96 KHz
- 2 synchronous I²S / AC-link output data stream pairs
- 2 synchronous I²S / AC-link input data stream pairs
- Multi-channel AC-link supported alternatively
- Integrated S/PDIF transmitter with IEC958 line driver
- Digital loopback and stream routing mechanism
- Peak meters on all streams
- MPU-401 MIDI UART port
- ACPI and PCI PMI support
- I²C subset interface peripherals control
- 16-pin, direct access GPIO port
- Windows® WDM drivers
- 24.576 and 22.5792 MHz crystal operation
- 3.3V operating supply (5V tolerant I/O)
- 128-Pin PQFP (14 x 20mm body)

1.1 Applications

- “Pro-sumer” audio
- High Fidelity audio reproduction
- PC-based Home Theater
- PC-based multi-channel audio like DVD-Audio
- PC-based multi-track audio recording
- General purpose multi-channel I/O
- PC-based data acquisition
- PC-based waveform generation
- PC-based instrumentation

Overview

The Envy24*PT*™ is a versatile PCI 24bit multi-channel audio controller that brings your computer at par with the fidelity of state-of-the-art home audio electronics. It allows up to 8 outbound streams and 4 simultaneous inbound channels. All paths in I²S mode pass 24-bit audio, "as is", unaltered, bit-per-bit accurate. Some of the typical applications for this part are computer based high fidelity multi-channel audio, home theater and entertainment, cost effective multi-track audio, PC-based data acquisition, waveform generation. To maintain a full digital path for PCM or compressed audio formats, the Envy24*PT* integrates a complete S/PDIF transmitter. The 2 output and 2 input pins can be combined with professional grade I²S converters, S/PDIF receivers or multi-channel out AC-link codecs, such as the VT1616™.

The Envy24*PT* supplies a master I²C interface providing peripherials control.

The Envy24*PT* integrates an independent MPU-401 MIDI UART.

Direct access GPIOs brings flexibility for multi-purpose use.

The Envy24*PT* is ACPI compliant making it suitable for platforms designed to be instantly on.

Depending on the sampling rates that need to be supported by the target solution, one or two crystals are sufficient to operate the whole system. For more detail on the part, please refer to the system block diagram Figure 4-1 in Section 4.

Pinouts

The following section includes the pinout diagram of the chip that is housed in a standard 128-PQFP. Also, three lists of pin assignments are provided for your convenience. They are logically sorted by functionality and description, alphabetically and numerically sorted in ascending order. These lists are provided to assist hardware development, test, debugging and quality assurance. Package specifications can be found in the Mechanical Specifications section.

2.1 Pinout Diagram

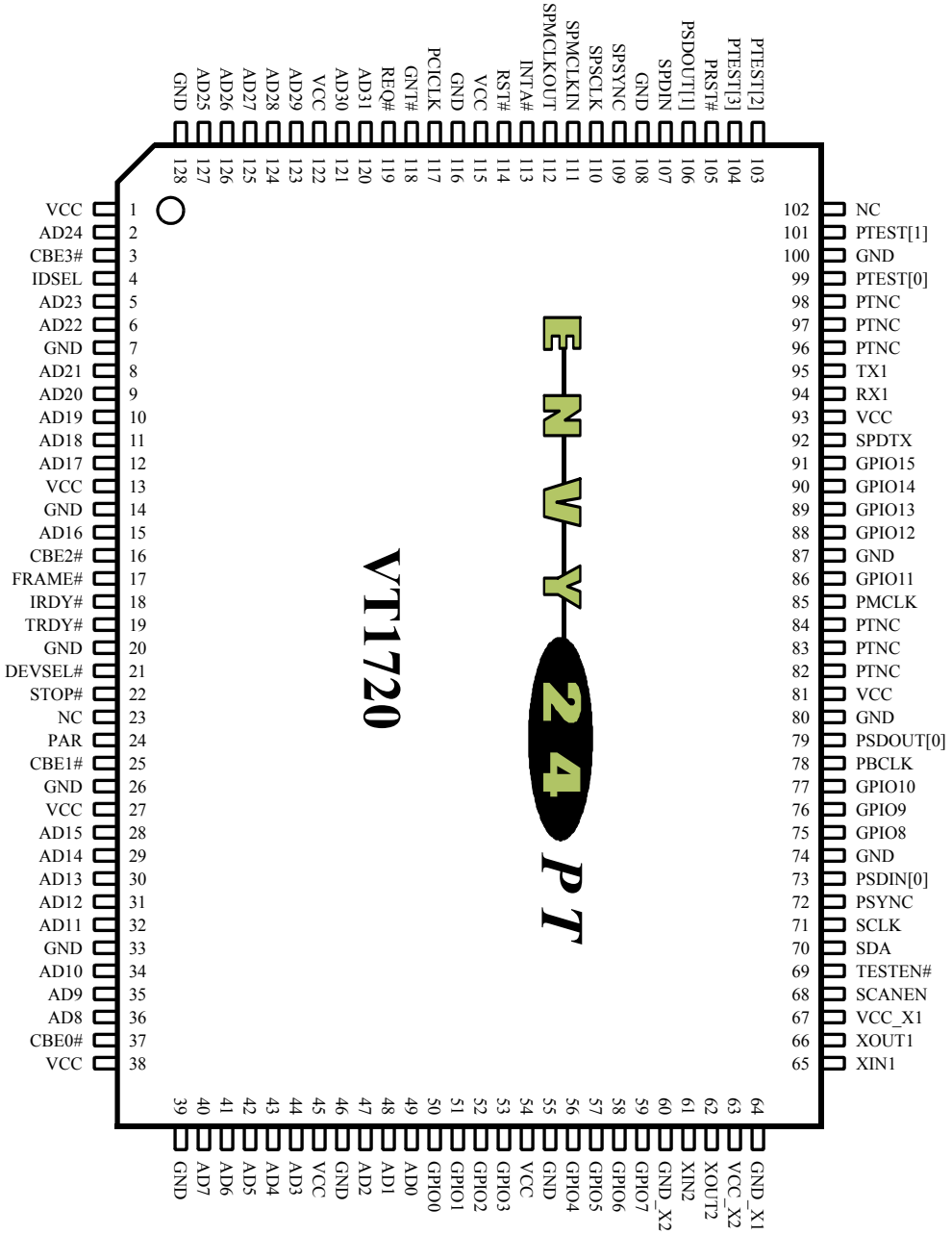


Figure 2-1. Pin Diagram

2.2 Pin Descriptions

The following table provides a brief description of each pin of the VT1720. Pins with dual usage may be listed twice for consistency. Please note that all PCI bus pins are 5V tolerant.

The following abbreviations are used to identify pin types.

I - Input Signal
O - Output Signal
B - Bidirectional Signal
OD - Open Drain
A - Analog Signal
PU - Pull-up. 50 KΩ nominal

Table 2-1. Pin Descriptions

PCI BUS INTERFACE		
Symbol	**Type**	**Description**
AD[31:0]	B	**Multiplexed PCI Address / Data Bus.**
CBE#[3:0]	B	**Bus Command / Byte Lane Enable.** These signals are bus commands during the address phase and byte lane enable during the data phase. These signals are output during a bus master cycle.
PCICLK	I	**PCI Bus Clock.**
DEVSEL#	B	**Device Select.** The VT1720 drives this signal active when it decodes its address as the current target of the current acces.
FRAME#	B	**PCI Cycle Frame.** When asserted by the bus mster, this signal indicates the beginning of a bus transaction.During the final data phase of a bus transaction it is deasserted.
GNT#	I	**PCI Bus Grant.** When active it indicates bus master is granted to the VT1720.
IDSEL	I	**Initialization Device Select.** This is the chip select during the PCI configuration register accesses
INTA#	OD	**PCI Interrupt Request.**
IRDY#	B	**Initiator Ready.**
PAR	B	**Parity.**
REQ#	O	**Bus Master Control Request.**
RST#	I	**System Reset.** All VT1720 registers and state machines are at default when this signal is asserted.
STOP#	B	**Target Disconnect.**
TRDY#	B	**Target Ready.**
I^2C PORT		
SDA	B	**Serial Data.**
SCLK	O	**Serial Bit Shift Clock.**
MPU-401 UART		
TX1	O, PU	**MPU-401 Transmit Data.**
RX1	I, PU	**MPU-401 Receive Data.**

Table 2-1. Pin Descriptions (continued)

PROFESSIONAL MULTI-TRACK AC-LINK / I²S INTERFACE		
Symbol	**Type**	**Description**
PSYNC	O	**Sync.** Sync (AC-Link Mode) or Left / Right Clock (I²S Mode) sample clock.
PBCLK	I/O	**Serial Bit Clock.** Typically output for I²S mode and input for AC-Link mode
PSDIN[0]	I	**Serial Data In.** Incoming stereo stream pair
PSDOUT[1:0]	O	**Serial Data Output.** 2 separate outbound stereo stream pairs. **PSDOUT[1]** can be used as S/PDIF out copy.
PMCLK	O	**Master Clock.** For AC'97 codecs or I²S converters
PRST#	O	**Cold Reset.** For I²S/AC-link converters
CLOCKS		
XOUT1	A	**Clock Out 1.**
XIN1	A	**Clock In 1.** 24.576 MHz (512*48 KHz). Runs the core blocks.
XOUT2	A	**Clock Out 2.**
XIN2	A	**Clock In 2.** 22.5792 MHz (512*44.1 KHz)
S/PDIF (SONY / PHILIPS DIGITAL INTERFACE)		
SPMCLKIN	I	**S/PDIF Master Clock Input.** Or other 128x or 256x clock for slave operation
SPMCLKOUT	O	**S/PDIF Master Clock Output.** 128x
SPSCLK	O	**S/PDIF Serial Bit Clock.**
SPDIN	I	**S/PDIF Serial Data In.**
SPDTX	A, PU	**S/PDIF IEC958 Line Driver Output.** The voltage divider implemented on the board will pull down signaling that the digital audio transmitter is implemented via bit CCS07[6]. Capable of driving 6mA.
SPSYNC	O	**S/PDIF Frame Sync.**
GENERAL PURPOSE I/O		
GPIO[15:1]	B, PU	**General Purpose I/O.** Capable of driving 8mA.
GPIO0 / I²S#	B, PU	**General Purpose I/O.** Sets AC-link interface for professional section during power-up (default). The state is reflected on CCS05[7] bit in reverse polarity. Capable of driving 8mA.
TEST MODE		
TESTEN#	I, PU	**Test Mode Enable.** Do not connect for normal operation.
SCANEN	I, PU	**Scan Test Mode Enable.** Must be grounded for normal operation.
PTEST[3:0]		**Internal Test Pins.** Do not connect for normal operation.
PTNC		**No Connect.**
NC		**No Connect.**
POWER AND GROUND		
VCC		**Digital Supply Voltage.** 3.3V
GND		**Ground.**

2.3 Pin Lists

Table 2 lists all the pins alphabetically. **Table 3** lists all the pins in numerical order.

Table 2-2. Alphabetical Pin Listing

Symbol	Pin(s)	Symbol	Pin(s)
AD[31:0]	2, 5-6, 8-12, 15, 28-32, 34-36, 40-44, 47-49, 120-121, 123-127	RX1	94
CBE#[3:0]	3, 16, 25, 37	SCANEN	68
DEVSEL#	21	SCLK	71
FRAME#	17	SDA	70
GNT#	118	SPDIN	107
GPIO[0] / I²S#	50	SPDTX	92
GPIO[15:1]	51-53, 56-59, 75-77, 86, 88-91	SPMCLKIN	111
IDSEL	4	SPMCLKOUT	112
INTA#	113	SPSCLK	110
IRDY#	19	SPSYNC	109
NC	23, 102	STOP#	22
PAR	24	TESTEN#	69
PBCLK	78	TRDY#	19
PCICLK	117	TX1	95
PMCLK	85	VCC	1, 13, 27, 38, 45, 54, 81, 93, 115, 122
PRST#	105	VCC_X1	67
PSDIN0	73	VCC_X2	63
PSDOUT[1:0]	79, 106	GND	7, 14, 20, 26, 33, 39, 46, 55, 74, 80, 87, 100, 108, 116, 128
PSYNC	72	GND_X1	64
PTEST[3:0]	99, 101, 103-104	GND_X2	60
PTNC	82-84, 96-98	XIN[2:1]	61, 65
REQ#	119	XOUT[2:1]	62, 66
RST#	114		

Table 2-3. Numerical Pin Listing

Pin #	Symbol	Pin #	Symbol	Pin #	Symbol	Pin #	Symbol
1	VCC	33	GND	65	XIN1	97	PTNC
2	AD24	34	AD10	66	XOUT1	98	PTNC
3	CBE3#	35	AD9	67	VCC_X1	99	PTEST[0]
4	IDSEL	36	AD8	68	SCANEN	100	GND
5	AD23	37	CBE0#	69	TESTEN#	101	PTEST[1]
6	AD22	38	VCC	70	SDA	102	NC
7	GND	39	GND	71	SCLK	103	PTEST[2]
8	AD21	40	AD7	72	PSYNC	104	PTEST[3]
9	AD20	41	AD6	73	PSDIN[0]	105	PRST#
10	AD19	42	AD5	74	GND	106	PSDOUT[1]
11	AD18	43	AD4	75	GPIO8	107	SPDIN
12	AD17	44	AD3	76	GPIO9	108	GND
13	VCC	45	VCC	77	GPIO10	109	SPSYNC
14	GND	46	GND	78	PBCLK	110	SPSCLK
15	AD16	47	AD2	79	PSDOUT[0]	111	SPMCLKIN
16	CBE2#	48	AD1	80	GND	112	SPMCLKOUT
17	FRAME#	49	AD0	81	VCC	113	INTA#
18	IRDY#	50	GPIO[0]	82	PTNC	114	RST#
19	TRDY#	51	GPIO[1]	83	PTNC	115	VCC
20	GND	52	GPIO[2]	84	PTNC	116	GND
21	DEVSEL#	53	GPIO[3]	85	PMCLK	117	PCICLK
22	STOP#	54	VCC	86	GPIO11	118	GNT#
23	NC	55	GND	87	GND	119	REQ#
24	PAR	56	GPIO[4]	88	GPIO12	120	AD31
25	CBE1#	57	GPIO[5]	89	GPIO13	121	AD30
26	GND	58	GPIO[6]	90	GPIO14	122	VCC
27	VCC	59	GPIO[7]	91	GPIO15	123	AD29
28	AD15	60	GND_X2	92	SPDTX	124	AD28
29	AD14	61	XIN2	93	VCC	125	AD27
30	AD13	62	XOUT2	94	RX1	126	AD26
31	AD12	63	VCC_X2	95	TX1	127	AD25
32	AD11	64	GND_X1	96	PTNC	128	GND

PCI Interface and Configuration Registers

Table 3-1. PCI Host Interface Register Map

Byte 3	Byte 2	Byte 1	Byte 0	Offset (Hex)
Device Identification		Vendor Identification		00
PCI Device Status		PCI Command		04
Class Code		Reserved. Read as 0	Revision ID	08
BIST	Header Type	Latency Timer	Reserved. Read as 0	0C
Controller I/O Base Address				10
Multi-Channel I/O Base Address				14
-				18
-				1C
Subsystem ID		Subsystem Vendor ID		2C
Reserved. Read as 0				30
Capability Pointer				34
Reserved. Read as 0				38
Minimum Latency and Maximum Grant		Interrupt Pin and Line		3C
	SVID Mask			40
Hardware Configuration Control				60
Power Management Capability		Next Item Pointer	Capability ID	80
PMCSR Support Extensions and Data		Power Management Control and Status		84

3.1 Envy24*PT* PCI Configuration Registers

PCI00: Vendor Identification

Address Offset: 00 - 01h

Default Value: 1412h

Bit	Attribute	Description
15:0	RO	Vendor Identification Number. This is the 16-bit value assigned to VIA Technologies, Inc.

PCI02: Device Identification

Address Offset: 02 - 03h

Default Value: 1724h

Bit	Attribute	Description
15:0	RO	Device Identification Number. 1724 reflects the parent part number.

PCI04: PCI Command

Address Offset: 04 - 05h

Default Value: 0000h

Bit	Attribute	Description
15:10	R0b	Reserved. Read as 0s.
9	R0b	Fast Back-to-Back Enable. This bit is hardwired to 0 (Not Implemented).
8	R/W	SERR# enable. Hardwired to 0 (Not Implemented).
7	R0b	A/D stepping enable. This bit is hardwired to 0 (Not Implemented).
6	R0b	Parity error detect enable. Hardwired to 0 (Not Implemented).
5	R0b	VGA palette snoop enable. Hardwired to 0 (Not Implemented).
4	R0b	Memory write and invalidate enable. Hardwired to 0 (Not Implemented).
3	R0b	Special Cycle Enable (SCE). Hardwired to 0 (Not Implemented).
2	R/W	Bus master enable. 1=enable. 0=disable (default).
1	R0b	Memory Access. Hardwired to 0 (Not Implemented).
0	R/W	I/O Space accesses enable. 1=enable. 0=disable (default).

PCI06: PCI Status

Address Offset: 06 - 07h

Default Value: 0210h

Bit	Attribute	Description
15	R/W/C	PAR status. Parity error detected (even when parity not enabled).
14	R/W/C	SERR# status. Read as 0 (Not Implemented).
13	R/W/C	Master abort status. This bit is set to 1 when master aborts and cleared by writing "1" to it.
12	R/W/C	Received target abort status. This bit is set to 1 when target abort is received and cleared by writing a 1 to it.
11	R0b	Signaled target abort status. This bit is set when target abort generated and cleared by writing a 1 to it. Hardwired to 0 (never abort).
10:9	R10b	DEVSEL# timing status. Envy24 always asserts DEVSEL# with medium timing.
8	R0b	PERR# response. Read as 0 (Not Implemented).
7	R0b	Fast back to back. Read as 0 (Not implemented).
6	R0b	User Define Function (UDF). Read as 0 (Not implemented).
5	R0b	Reserved. Read as 0. 33MHz only.
4	R1b	Hardwired to 1 to indicate the support for PCI power management capability.
3:0	R0000b	Reserved. Read as 0s.

PCI08: Revision ID

Address Offset: 08h - 09h

Default Value: 000Xh

Bit	Attribute	Description
15:0	R00h	-
7:0	RO	Revision ID

PCI0A: Class Code

Address Offset: 0Ah - 0Bh

Default Value: 0401h

Bit	Attribute	Description
15:8	RO	Base Class. Reflects Multimedia
7:0	RO	Sub class. Reflects Audio.

PCI0C: Cache Size

Address Offset: 0Ch

Default Value: 00h

Bit	Attribute	Description
7:0	RO	Read as 0. Not supported

PCI0D: Latency Timer

Address Offset: 0Dh

Default Value: 00h

Bit	Attribute	Description
7:3	R/W	Latency timer
2:0	RO	Read as 0

PCI0E: Header Type

Address Offset: 0Eh

Default Value: 00h

Bit	Attribute	Description
7:0	RO	Read as 0

PCI0F: BIST

Address Offset: 0Fh

Default Value: 00h

Bit	Attribute	Description
7:0	RO	Read as 0. Not supported

PCI10: Envy24PT I/O Base

Address Offset: 10h - 13h

Default Value: 00000001h

Bit	Attribute	Description
31:5	RW	Controller I/O Base Address for CCSxx registers described in chapter 4
4:1	R0h	Hardwired to 0 to have 32 bytes I/O space. This includes the MIDI UART.
0	R1b	Hardwired to 1 to indicate registers map to I/O space

PCI14: Multi-Channel I/O Base

Address Offset: 14h -17h

Default Value: 00000001h

Bit	Attribute	Description
31:7	R/W	Multi-Channel I/O Base Address for MTxx registers described in chapter 4
6:1	R0	Hardwired to 0 to have 128 bytes I/O space
0	R1b	Hardwired to 1 to indicate registers map to I/O space

PCI2C: Sub-Vendor ID

Address Offset: 2Ch - 2Fh

Default Value: 17241412h

Bit	Attribute	Description
31:0	RO	Sub-vendor ID: Read it from external E²PROM after reset if it exists, otherwise, same as vendor ID. It can also be written by disabling write protection bit defined in PCI42_7.

PCI34: Capability Pointer

Address Offset: 34h

Default Value: 80h

Bit	Attribute	Description
7:0	RO	CP7-CP0: Capability data structure pointer for PCI power management. Hardwired to 80h.

PCI3C: Interrupt Pin and Line

Address Offset: 3Ch - 3Dh

Default Value: 01FFh

Bit	Attribute	Description
15:8	RO	01h read from this register indicates the interrupt pin used is INTA# and cannot be modified.
7:0	R/W	Interrupt line routing information set by POST during power-up initialization. Default FFh indicates no connection to the PIC yet.

PCI3E: Latency and Grant

Address Offset: 3Eh - 3Fh

Default Value: 0000h

Bit	Attribute	Description
15:8	RO	Maximum latency
7:0	RO	Minimum grant

PCI42: Subsystem ID Mask

Address Offset: 42h

Default Value: 0000h

Bit	Attribute	Description
		Reserved
7	R/W	0: SVID read only. (default) 1: SVID read/write enable.

PCI80: Capability ID

Address Offset: 80h

Default Value: 01h

Bit	Attribute	Description
7:0	RO	Capability ID

PCI81: Next Item Pointer

Address Offset: 81h

Default Value: 00h

Bit	Attribute	Description
7:0	RO	Hardwired to 0 to indicate the end of list

PCI82: Power Management Capabilities

Address Offset: 82h - 83h

Default Value: 0401h

Bit	Attribute	Description
15:11	RO	PME not supported. Hardwired to 0.
10	R1	D2 state support. Hardwire to 1.
9	R0	D1 state not support. Hardwired to 0.
8:6	R000	Reserved.
5	R0	DSI. Hardwired to 0.
4	R0	Aux. Power. Hardwired to 0
3	R0	PMC clock for generation of PME#. Hardwired to 0.
2:0	R001b	Hardwired to 001 to indicate PPMI 1.0 compliance

PCI84: Power Management Control and Status

Address Offset: 84h - 85h

Default Value: 0000h

Bit	Attribute	Description
15	R0b	PME status. Read as 0.
14:13	R00b	Data scale. Not supported.
12:9	R0h	Data select: Not supported.
8	R0b	PME assertion. Hardwired to 0
7:2	RO	Hardwired to 000000
1:0	R/W	Power state. To determine the current state of power state. 00 : D0 01 : D1 (not supported) 10 : D2 11 : D3_hot

There are four power states defined in the PCI bus power management spec.

States	Description
D0	Normal operation state after system power up or internal reset
D1	not supported.
D2	Power down all the blocks defined in the power down registers.
D3(hot)	Same as D2 state, except a transition to D0 will generate an internal reset (incl. PCI config. space)

PCI86: PMCSR Base and Data

Address Offset: 86h - 87h

Default Value: 0000h

Bit	Attribute	Description
15:0	R0000h	-

Hardware Interface Registers

In the previous section PCI host interface and configuration registers were discussed. In this section description of the major blocks, their respective hardware interfaces and associated registers will be discussed.

The first figure in this section, **Figure 4-1**, is a chip level block diagram with typical external interface usage. It is a very good overview of the whole chip, but should not be regarded as the most detailed diagram. As appropriate, the databook will resort to sub-block diagrams to further detail the functionality.

The following descriptive summary can be considered along with **Figure 4-1**. The DMA engine is to be programmed via MT19 (and other supporting registers) to configure DMA operation for a single 6 audio channel interleaved DMA, or to breakup the assignments into 4 or 2 audio channel interleaved operation, which allows the unassigned audio channels to be configured as individual stereo pair DMAs. There is a dedicated stereo DMA for the integrated S/PDIF transmitter, the same data is available on an I2S pin.

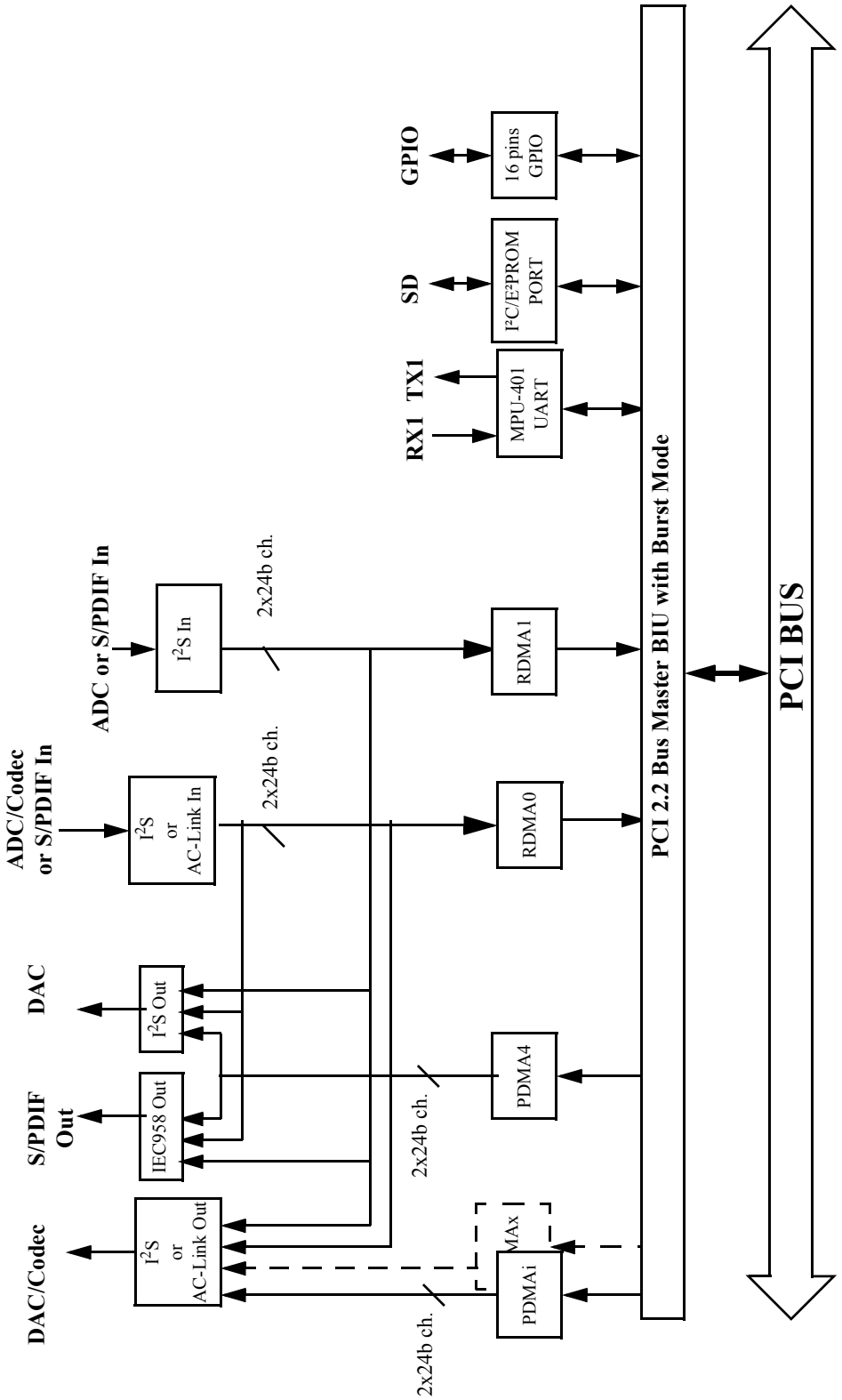


Figure 4-1. Functional Block Diagram

4.1 Controller Registers

The following registers are offset from base address set by PCI10. The 32-byte I/O space includes main control/status registers, I^2C interface and MPU-401 MIDI UART registers. Each CCSxx register is physically located at the address determined by [PCI10]+xx and accessed directly. The registers can be accessed as a Byte, Word or DWord.

Table 4-1. CCSxx Controller Register Map

Byte 3	Byte 2	Byte 1	Byte 0	Offset (Hex)
-	Envy24PT Status	Interrupt Mask	Global	00
S/PDIF Configuration	I²S Configuration	AC-link Configuration	System Configuration	04
RX UART queue	TX UART queue	-		08
-	UART Setting	UART Comm./Status	MIDI UART Data	0C
I²C Port Control/Status	I²C Port R/W Data	I²C Port Byte Address	I²C Port Dev. Address	10
GPIO[15:0] Write Mask Register		GPIO[15:0] Data Register		14
-		GPIO[15:0] Direction Register		18
-		-	Power Down	1C

CCS00: Control / Status

Address Offset: 00h

Default Value: 00h

Bit	Attribute	Description
7	R/W	**Entire Chip Soft Reset**. To reset, write "1", then write "0" to restore normal operation. When reset, all registers revert to their default values, except all PCI configuration registers plus CCS00 (this register) and CCS04-07. The EEPROM (if populated and indicated as so via GPIO[3]) data is read into the effected registers, including the SubVendor ID. When this bit is written to 1, then back to zero, a corresponding reset sequence also occurs on the PRST# output pin.
6:0	R/W	**Reserved**

CCS01: Interrupt Mask

Address Offset: 01h

Default Value: FEh

Bit	Attribute	Description
7	R/W	**MPU-401 MIDI UART Receive Interrupt Mask**. See CCS0E for high watermark setting.
6	R/W	**Reserved**
5	R/W	**MPU-401 MIDI UART Transmit Interrupt Mask**. See CCS0E for low watermark setting.
4	R/W	**Multi-Channel Playback and Record**. This is the macro interrupt mask for any P and RDMAx.
3:0	R/W	**Reserved**

CCS02: Interrupt Status

Address Offset: 02h

Default Value: 00h.

These bits are sticky and only writing a 1 to that bit location will clear itself.

Bit	Attribute	Description
7	R/W/C	**MPU-401 MIDI UART Receive FIFO**
6	R/W	**Reserved**
5	R/W/C	**MPU-401 MIDI UART Transmit FIFO**
4	RO	**Multi-Channel Playback or Record**. This is the macro interrupt status for any PDMAx and RDMAx. To clear individual status bit, write a 1 to the associated bit location defined in section 4.2, MT00.
3:0	R/W	**Reserved**

CCS04: System Configuration

Address Offset: 04h

Default Value: 0Fh

The following four bytes (04h-07h) have to be read from E^2PROM by driver and then written to setup the codec configuration, unless otherwise noted.

Bit	Attribute	Description
7:6	R/W	**XIN1 Clock Source Configuration**. Refer to register MT01. 00: XIN1: 24.576MHz crystal (96 KHz*256) 01: Reserved 1x: Reserved
5	R/W	1: MPU-401 UART implemented 0: MPU-401 UART not implemented.
4	R/W	**Reserved**
3:2	R/W	**Physical Input Configuration** 00: one stereo ADC connected 01: two stereo ADCs connected 10: one stereo ADC and a S/PDIF receiver connected 11: No physical inputs
1:0	R/W	**Physical Output Configuration** 00: one stereo DAC connected 01: two stereo DACs connected 10: Reserved 11: Reserved Must have at least one stereo pair DAC.

CCS05: AC-Link Configuration

Address Offset: 05h

Default Value: 00h

Except for bit-7, the four bytes at CCS04 should be read from E^{2}PROM by driver and then written to setup the codec configuration.

Bit	Attribute	Description
7	R/W	**Multi-Channel Converter Type**. 0: AC'97 1: I²S. Reflects power-up status of pin 50 during reset cycle in reverse polarity. Can be overwritten.
6:2	R/W	**Reserved**.
1	R/W	**SDATA_OUT Mode** 0: Reserved. 1: AC-Link Packed Mode. AC'97 codec SDATA_OUT packed in slots per AC'97 2.2 spec only on PSDOUT0 (pin79). See VT1616 spec as the codec to be used in this mode. If bit-7 is 0, i.e. AC'97 mode, it may affect the DMA to pin mappings where the audio streams are transferred to. See description in MT05[1:0] and **Table 4-3**.
0	R/W	**Reserved**.

CCS06: I^{2}S Converters Features

Address Offset: 06h

Default Value: 01h

This byte is valid only when CCS05[7] is 1. The four bytes at CCS04 should be read from E^{2}PROM by driver and then written to setup the codec configuration.

Bit	Attribute	Description
7	R/W	**I²S Codec Volume and Mute** 0: I^{2}S codec has no volume/mute control feature. 1: I^{2}S codec has volume/mute control capability and need to be program through GPIO (e.g., CS4222)
6	R/W	**I²S Converter 96 KHz Sampling Rate Support**. 0: Not supported; 1: Supported
5:4	R/W	**Converter Resolution** 00: 16-bit 01: 18-bit 10: 20-bit 11: 24-bit
3	R/W	**I²S Converter 192 KHz Sampling Rate Support**. 0: Not supported; 1: Supported
2:0	R/W	**Other I²S IDs**

CCS07: S/PDIF Configuration

Address Offset: 07h

Default Value: 01h

The four bytes at CCS04 should be read from E^2PROM by driver and then written to setup the codec configuration.

Bit	Attribute	Description
7	R/W	1: Enable integrated S/PDIF transmitter. Valid only when bit 6 of this register is '1'. Must be disabled to change mode via MT3C.
6	R/O	1: Internal S/PDIF Out implemented. Reflects the state of pin 92, SPDTX during reset. If '0', the transmitter is not implemented on the board. Note that it is reverse polarity of pin 92 reset state.
5:2	R/W	S/PDIF Chip IDs
1	R/W	1: S/PDIF Stereo In is present.
0	R/W	1: S/PDIF Out is present. This bit must be "1" to activate the S/PDIF output.

CCS0A: UART TX FIFO Queue Status

Address Offset: 0Ah

Default Value: 00h

Description: This read-only register reflects the number of valid bytes in hex form, ready to be transmitted on TX1 (pin95) from the TX FIFO. The UART FIFO is 32bytes deep in each direction.

Bit	Attribute	Description
7:5	RO	Reserved.
4:0	RO	Valid MPU-401 data bytes in TX FIFO.

CCS0B: UART RX FIFO Queue Status

Address Offset: 0Bh

Default Value: 00h

Description: This read-only register reflects the number of valid bytes hex form, to be read by the host from the RX FIFO. The UART FIFO is 32bytes deep in each direction.

Bit	Attribute	Description
7:5	RO	Reserved.
4:0	RO	Valid MPU-401 data bytes in RX FIFO.

CCS0C: MIDI UART Data

Address Offset: 0Ch

Default Value: 00h

Bit	Attribute	Description
7:0	R/W	MIDI UART data register

CCS0D: MIDI UART Command / Status

Address Offset: 0Dh

Default Value: 00h

Description: UART Command / Status bits are defined according to the table below. This is an implementation that exhibits some deviation from the MPU-401 defacto standard in order to support interrupt handling of receive data. Write "1" to bit-0 to enter UART mode. It is not neccessary to read back the acknowledge byte. Bits 1 through 4 reflect the state of the transmit and receive FIFOs as defined below.

Bit	Attribute	Description
7:1	W	Command Register - Reserved
0	W	Command Register - UART (1) / Standalone (0) Mode Select
7:5	R	Status Register - Reserved
4	R	Status Register - Rx FIFO Full
3	R	Status Register - Rx FIFO Empty
2	R	Status Register - Tx FIFO Full
1	R	Status Register - Tx FIFO Empty
0	R	Status Register - UART (1) / Standalone (0) Mode

CCS0E: UART Setting

Address Offset: 0Eh

Default Value: 00h

Description: This register allows setting high/low watermarks for RX/TX FIFO interrupts to avoid polling or constant interruption during heavy system activity. The UART FIFO is 32bytes deep in each direction.

Bit	Attribute	Description
7:6	R/W	Reserved.
5	R/W	1: Receive FIFO high watermark setting. 0: Transmit FIFO low watermark setting.
4:0	R/W	Enter the watermark value, between 0 and 31 (00h to 1Fh). Both RX and TX FIFO are 32-bytes. The default watermark level is 0 for both TX and RX.

CCS10: I²C Port Device Address

Address Offset: 10h

Default Value: 00h

Each write to this register will trigger to start the read/write cycle. So, before write to this I/O address, driver needs to check to make sure that the status bit is idle as defined in the I²C status register CCS13. The controller is always the only master and does not support multi-byte data burst mode.

Bit	Attribute	Description
7:1	R/W	I²C device address. Device address "1010000" is reserved for the external I²C E2PROM such as 24C02 for sub-vendor ID and configuration data.
0	R/W	0: read 1: write

CCS11: I²C Port Byte Address

Address Offset: 11h

Default Value: 00h

Bit	Attribute	Description
7:0	R/W	Byte address to read or write

CCS12: I²C Port Read / Write Data

Address Offset: 12h

Default Value: 00h

Bit	Attribute	Description
7:0	RW	Read or write data

CCS13: I²C Port Control and Status

Address Offset: 13h

Default Value: 00h

When bit 0 is 0 (meaning the I²C port is idle), SCLK (pin 71) will be tri-stated. Envy24PT is providing the serial clock only when it reads/writes through I²C bus at a nominal rate of 31.25 KHz.

Bit	Attribute	Description
7	RO	Reflects the power strapping on GPIO3 (pin 53). A 1 (default) indicates external E²PROM exists. A 0 (pull down by a resistor) means, no external E²PROM connected.
6:2	0	-
1	R/W	Reserved. Keep at 0 state.
0	RO	I²C port read/write status. 0: idle 1: busy

CCS14: GPIO Data

Index: 14 -15h

Default Value: 0000h

The direction is set up in CCS18, the GPIO direction control register (see CCS1E for MSB GPIO Data Register). These register bits can be writable only when the corresponding mask bit is zero in the mask register, CCS16. If the direction is output, it reads back the last data written. The use of these will depend upon board configuration as defined by the E²PROM settings content. See CCS04 register description for more details.

Bit	Attribute	Description
15:0	R/W	GPIO data (Warning: few GPIO pins may be shared with other functions)

CCS16: GPIO Write Mask

Index: 16 - 17h

Default Value: FFFFh

Bit	Attribute	Description
15:0	R/W	GPIO15 through GIO0 write mask 0: Corresponding CCS14 register bit can be written. 1: Can NOT be written.

CCS18: GPIO Direction Control

Index: 18h - 1Ah

Default Value: 000000h

Bit	Attribute	Description
15:4	R/W	GPIO15 through GPIO4 direction.
3	R/W	GPIO3 direction. During reset, this pin is used for E²PROM power-on strapping.
2	R/W	GPIO2 direction. If TESTEN# pin is active, this pin is always input.
1:0	R/W	GPIO1 and GPIO0 direction.

For all bits 0: input; 1: output.

CCS1C: Power Down

Index: 1Ch

Default Value: 00h

Bit	Attribute	Description
7	R/W	1: Crystal clock generation power down for XTAL_1
6	R/W	Reserved
5	R/W	1: Crystal clock generation power down for XTAL_2
4	R/W	1: Stop I²C port clock
3	R/W	1: Stop MIDI clock
2	R/W	1: Stop S/PDIF clock
1	R/W	Reserved.
0	R/W	1: Stop Multi-channel I²S serial interface clock

4.2 Multi-Channel Control Registers

The following registers are offset from base address set by PCI14. The MTxx registers are located at [PCI14]+xx. The 128-byte I/O space controls the multi-channel record and playback, audio stream routing and related output capability. Refer to the introduction of this chapter for a concise description of the DMA channels involved.

Table 4-2. MTxx Controller Register Map

Byte 3	Byte 2	Byte 1	Byte 0	Offset (Hex)
DMA Interrupt Mask	I²S data format	Sampling Rate Select.	DMA Interrupt Status	00
AC '97 Data Port		AC '97 Comm./Stat.	AC '97 Index	04
-				08
-				0C
Interleaved Playback DMA (PDMAi) Current/Base Address				10
-	PDMAi Current/Base Count			14
Global DMA Pause/R.	Underrun/Overrun	PDMAi Burst Size	Global DMA Start/Stop	18
-	PDMAi Current/Base Terminal Count			1C
Record DMA 0 (RDMA0) Current/Base Address				20
Record DMA 0 Current/Base Terminal Count		Record DMA 0 Current/Base Count		24
-				28
Routing control to PSDOUT[0] and PSDOUT[1]				2C
Record DMA 1 Current/Base Address				30
Record DMA 1 Current/Base Terminal Count		Record DMA 1 Current/Base Count		34
-				38
Peak meter data	Peak meter index	S/PDIF IEC958 Control Register		3C
Playback DMA 4 (PDMA4)/ S/PDIF output Current/Base Address				40
PDMA4 Current/Base Terminal Count		PDMA4 Current/Base Count		44
Playback DMA 3 (PDMA3)/ S/PDIF output Current/Base Address				50
PDMA3 Current/Base Terminal Count		PDMA3 Current/Base Count		54
Playback DMA 2 (PDMA2)/ S/PDIF output Current/Base Address				60
PDMA2 Current/Base Terminal Count		PDMA2 Current/Base Count		64
Playback DMA 1 (PDMA1)/ S/PDIF output Current/Base Address				70
PDMA1 Current/Base Terminal Count		PDMA1 Current/Base Count		74

4.2.1 Multi-Channel Mode Registers

MT00: DMA Interrupt Status

Address Offset: 00h

Default Value: 00h

This register relates to both all DMA operation modes. When DMAs are stopped, the last latched value is retained. This "DC" value may affect the converters state.

Bit	Attribute	Description
7	R/W/C	SPDIF Out/PDMA4 pair playback interrupt status. Write a 1 to clear.
6	R/W/C	PDMA3 pair playback interrupt status. Write a 1 to clear.
5	R/W/C	PDMA2 pair playback interrupt status. Write a 1 to clear.
4	R/W/C	PDMA1 pair playback interrupt status. Write a 1 to clear.
3	R/W/C	DMA FIFO underrun/overrun condition. See MT1A for status.
2	R/W/C	RDMA1 (typically S/PDIF input) pair record interrupt status. Write a 1 to clear.
1	R/W/C	RDMA0 pair (typically ADC) record interrupt status. Write a 1 to clear.
0	R/W/C	Multi-channel interleaved/PDMA0 pair playback interrupt status. Write a 1 to clear.

MT01: Sampling Rate Select

Address Offset: 01h

Default Value: 00h.

Bits [3:0] specify the audio sample rate whenever the clock source is selected as Internal (XIN1 or XIN2) via bit 4. If the clock source is selected as External via bit-4 either a 256fs (required for AC-Link) or 128fs (optional for I2S) master clock must be supplied on the SPMCLKIN pin; MT02[3] is to be set accordingly, and the sample rate as well as the MCLK ratio are implicitly applied by the Envy24PT; the relationship between SPMCLKIN and PMCLK is always 1:1. If the clock source is set to Internal, the setting of MT02[3] specifies the ratio to be generated on PMCLK (divided down from the internal clock, or 1:1, as needed) as 256fs or 128fs (not applicable to AC-Link). However, 256fs is not available for any sample rate above 96 KHz for which the frequency available on XIN1 (48 KHz based rates) or XIN2 (44.1 KHz based rates) would be exceeded. Based upon the sample rate and MCLK/LRCLK ratio, the Envy24PT automatically derives SCLK and LRCLK to be output to the PBCLK and PSYNC pins always as 64fs and fs, respectively, for either internally or externally clocked I2S operation. See supporting text for details specific to AC-Link operation. See **Figure 4-3** and **Figure 4-4** on page 15 in this chapter.

Bit	Attribute	Description
7:5	R000b	**Reserved**
4	R/W	**S/PDIF Input Clock as Master**. 0: Disabled, 1: Enabled (Envy24PT slave mode) The S/PDIF receiver chip or other source provides the master clock through SPMCLKIN (pin 111). Note that in this mode, 256x is the highest master clock available while the AC'97 MCLK requires 512X. AC'97 codecs, such as the VT1611A are designed based on BCLK which uses MCLK/2, i.e. 256X. When S/PDIF provides the master clock, if VIA AC'97 codecs are used, before setting S/PDIF as the master clock, proceed to switching the primary codec into slave mode (refer to the MT05 description). In this mode PBCLK will be output from Envy24PT.
3:0	R/W	**Sample Rate Select for Internal Clock Operation**. The entire system runs synchronously, based on the same master clock and sampling rate. All channels are set to the same rate. These bits are ignored if S/PDIF input is master. See bit 4 of this register. 0000: 48 KHz (default) 0001: 24 KHz 0010: 12 KHz 0011: 9.6 KHz 0100: 32 KHz 0101: 16 KHz 0110: 8 KHz 0111: 96 KHz 1110: Reserved 1111: 64 KHz 1000: 44.1 KHz 1001: 22.05 KHz 1010: 11.025 KHz 1011: 88.2 KHz others: reserved

MT02: I²S Data Format

Address Offset: 02h

Default Value: 00h

Bit	Attribute	Description
7:4	RO	**Reserved**
3	R/W	**MCLK / LRCLK Ratio** 0: 256x (default) 1: 128x
2	R/W	**Reserved**
1:0	R/W	**Data Format** 00: I²S (timing diagram provided below) others: Reserved

See **Figure 4-2** below for a timing diagram for bits [1:0]. See **Figure 4-3** and **Figure 4-4** on page 15 and page 15 respectively for the visual description of other bits.

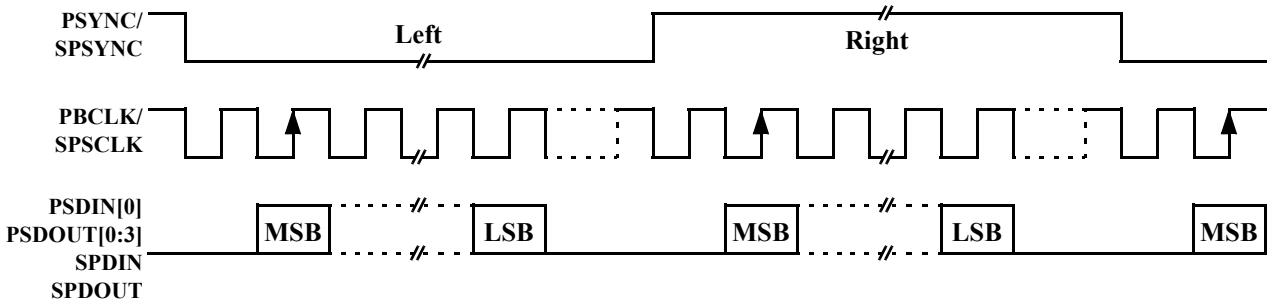


Figure 4-2. I²S Format Timing Diagram

MT03: DMA Interrupt Mask

Address Offset: 03h

Default Value: FFh

This register relates to all DMA channels. By default all interrupts are off (‘1’), i.e. masked. When enabled (set to ‘0’), MT00 interrupt status reflects each DMA channels interrupt state.

Bit	Attribute	Description
7	R/W	SPDIF Out/PDMA4 pair playback interrupt mask. Always valid.
6	R/W	PDMA3 pair playback interrupt mask. Valid only when MT19>00b.
5	R/W	PDMA2 pair playback interrupt mask. Valid only when MT19>01b.
4	R/W	PDMA1 pair playback interrupt mask. Valid only when MT19=11b.
3	R/W	DMA FIFO underrun/overrun condition interrupt mask. MT1A reports the offending channel.
2	R/W	RDMA1 (typically S/PDIF input) pair record interrupt mask. Always valid.
1	R/W	RDMA0 pair (typically ADC) record interrupt mask. Always valid.
0	R/W	Multi-channel interleaved/PDMA0 pair playback interrupt mask. Always valid.

MT04: AC’97 Codec Registers Index

Address Offset: 04h

Default Value: 00h

This register is valid when the AC-link interface (CCS05[7] = 0) is used. It has no validity when the converter interface is set to I²S mode (CCS05[7] = 1).

Bit	Attribute	Description
7	R0	-
6:0	R/W	AC’97 registers Index. Refer to the AC’97 specification for register descriptions.

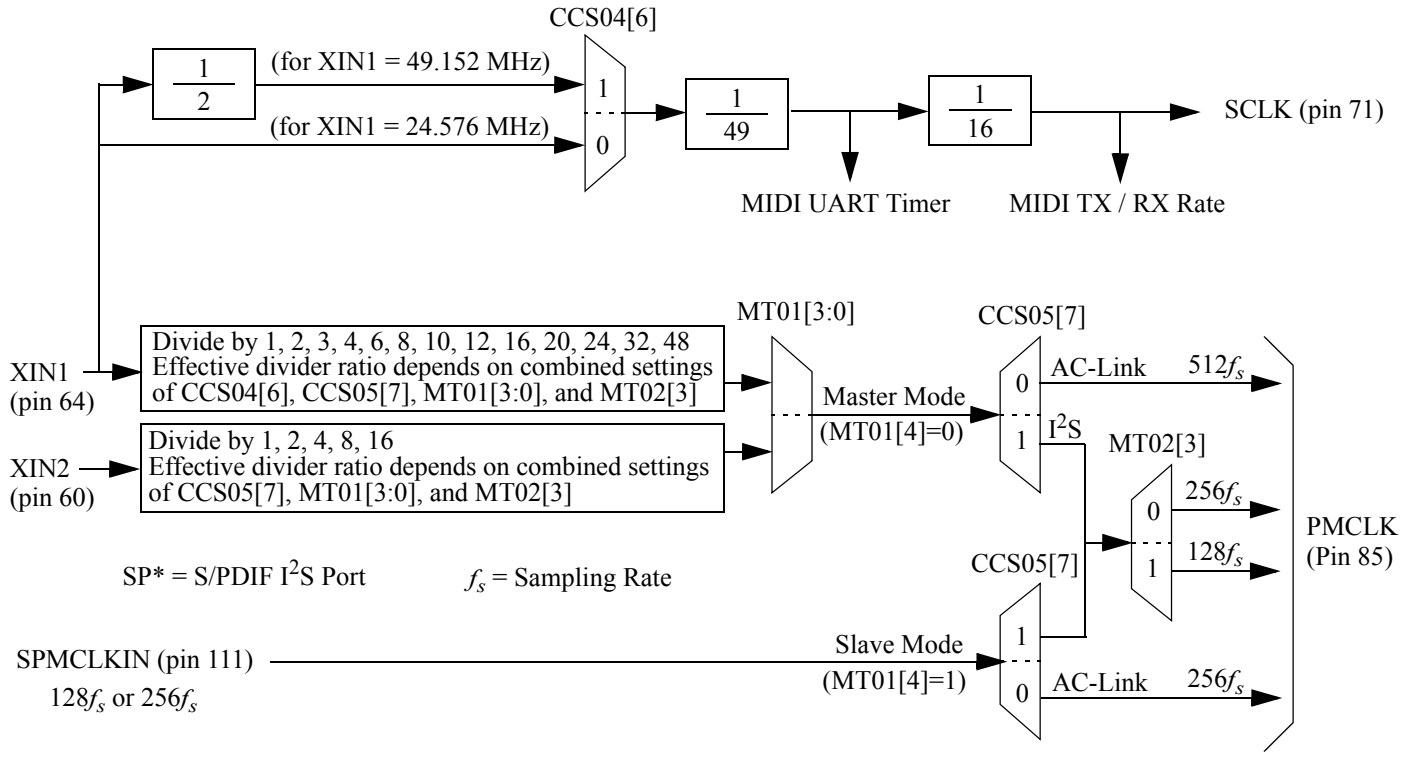


Figure 4-3. Crystals to Master Clocks Clock Generation Tree

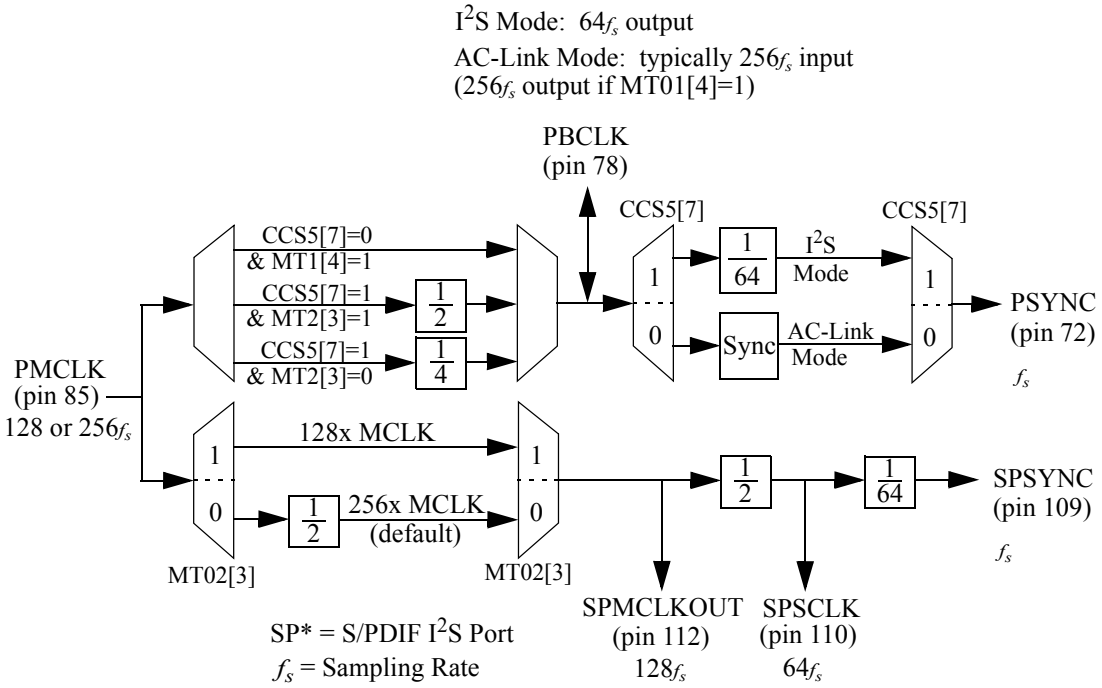


Figure 4-4. Master Clocks to Bit Clocks, L/R Clocks and Sync Generation

MT05: AC'97 Codecs Command and Status

Address Offset: 05h

Default Value: 00h

This register is intended for use when the audio interface is set to AC-link mode (CCS05[7] = 0). It has no meaning in I²S mode (CCS05[7] = 1), except that the function of bit-7 still applies. Bits 6 and 7 are used to support AC-Link mode operation under the condition of the clock source being supplied externally to the SPMCLKIN pin (must be 256fs). The codec is to operate in slave mode and accept input from the PBCLK pin, which will be equivalent to the SPMCLKIN source. The programming sequence to put the codec into slave mode is as follows: set bit 6 to assert PSYNC, set bit 7 while maintaining bit 6 set to cause the codec to sample the asserted PSYNC condition, reset both bits 6 and 7 to operate in slave mode. To return to master mode operation (PBCLK output by codec) perform a codec cold reset via bit 7.

Bit	Attribute	Description
7	R/W	**AC'97 Codec Cold Reset**. Write 1 to assert PRST# (pin105) active. Write 0 to restore normal operation.
6	R/W	**AC'97 Codec Warm Reset**. Write 1 to issue warm reset by asserting PSYNC (pin 72) high. This bit together with PRST# (pin 105) active (MT05[7]=1) can be used to set the external VIA primary AC'97 codec to slave mode (such as the VT1611A). This must be done when S/PDIF input is the master. Apply Cold reset to restore codec master mode.
5	R/W	**Initiate Codec Register Write Cycle**. Write 1 to write to AC'97 codec register. Reading a 1 indicates the write cycle is still in progress, cleared when write cycle complete.
4	R/W	**Initiate Codec Register Read Cycle**. Write 1 to read AC'97 codec register. Reading a 1 indicates the read cycle is still in progress, cleared when there is valid data.
3	RO	**AC'97 Codec Ready Status**. After power-on, check that this bit is 1 before accessing codec registers.
2	R0b	**Reserved**
1:0	R/W	**AC'97 Codec Select**. ID for external AC'97 register read/write when split mode (CCS05[1] = 0) is used. When a 6-channel AC'97 like the VT1616 is used (CCS05[1] = 1), multichannel PCM data is transmitted on the default slots but on the same data out pin, PSDOUT0, pin 79. 00: select primary AC'97 codec. PCM transmitted on time slots 3,4. 01: reserved. 10: reserved. 11: reserved.

MT06: AC'97 Codecs Data Port

Address Offset: 06h - 07h

Default Value: 00h

This register is valid when AC-link interface (CCS05[7] = 0) is used. It has no meaning when the converter interface is set to I²S mode (CCS05[7] = 1).

Bit	Attribute	Description
15:8	R/W	AC'97 codec register data high byte (index 07h) Refer to the AC'97 specification for register descriptions..
7:0	R/W	AC'97 codec register data low byte (index 06h). Refer to the AC'97 specification for register descriptions.

4.2.2 Multi-Channel Interleaved DMA Playback Registers

The following **Figure 4-5** represents the manner in which the data is sequenced and interleaved for efficient transfer of multi-channel data over the PCI bus. A total of 12 layers (or sample times t_0 through t_{11}) of deep buffer structure is implemented for a seamless flow of each stream, i.e. a maximum of 12 * 8chs * 24bit data can be buffered before the physical output pins. Each burst cycle fills 4 layers (or sample time t_x to t_{x+4}) for each channel. If empty time slots (or layers) remain, a new bus request is issued until all layers are full. An initial buffer fill therefore, generates 3 consecutive bus requests. 32-bit unpacked data transfers are used across the PCI bus regardless of the audio data resolution. All transfer data are left (MSB) justified. Each transfer request results in a PCI bus master burst cycle. The maximum and default burst size is 4 * 8chs = 32 PCI data cycles. The burst size can be reduced to 6, 4 or 2 channels (see MT19), i.e. shrink to 24, 16 or 8 PCI data cycles transferred. This improves PCI bus efficiency when only a limited amount of channels are used and frees up the DMA FIFO for independent stereo pair operation where each channel has independent control over the data flow.

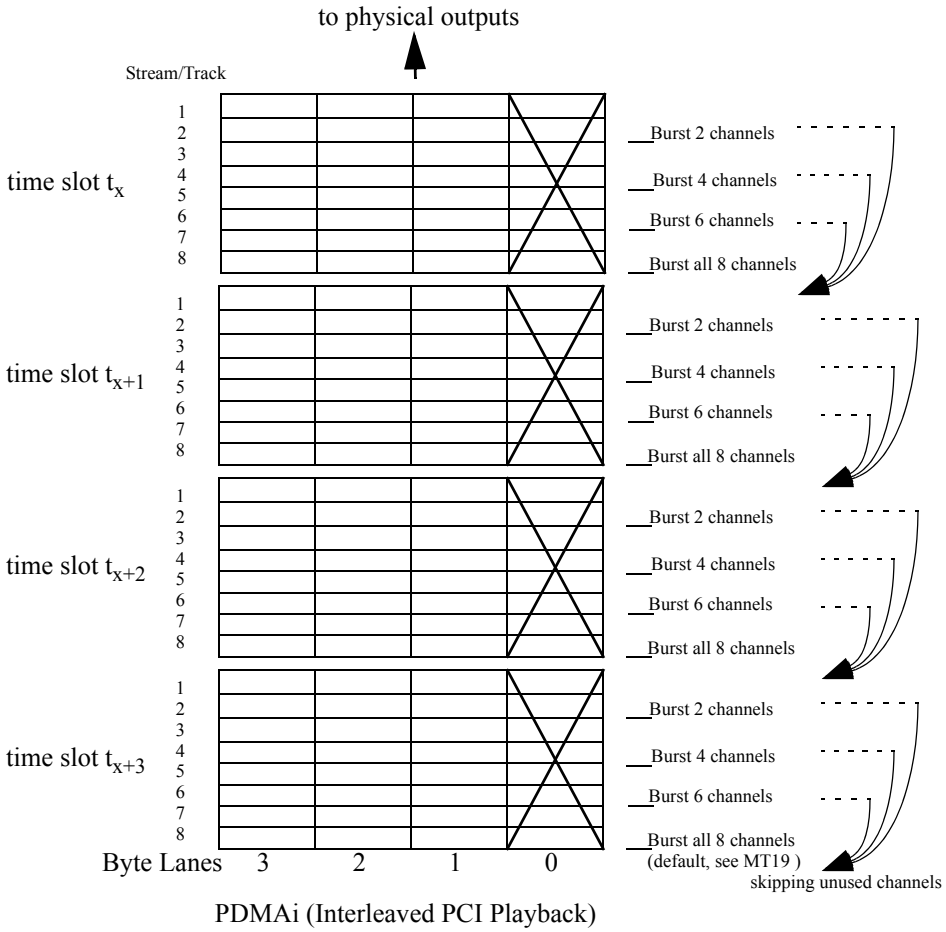


Figure 4-5. Multi-Channel Interleaved DMA Playback

The usage of I²S converters (see CCS05[7]) or AC-link (packed mode, see CCS05[1]) determines which DMA slots map into which physical pin. The table below shows the DMA FIFO mapping into I²S or AC-link time slots. Refer to **Figure 4-5** above for DMA stream/track information or **Figure 4-7** on page 27 of this chapter. The ID in AC'97 mode is the value read at the standard location 28h, along with the AMAP bit. The mapping of proper DMA FIFO track into corresponding time slots is done to eliminate the need for manipulation of streaming data by the software drivers per Microsoft WAVEFORMATEXTENSIBLE format and the definition of predetermined multichannel speaker location.

DMA FIFO track	I²S mode (CCS05[7]=1)	Packed AC-link (CCS05[1]=1)
PDMAi 1,2 or PDMA0	PSDOUT0 L/R	PSDOUT0 3,4 (Front L/R)
PDMAi 3,4 or PDMA1	-	PSDOUT0 6,9 (Center/LFE)
PDMAi 5,6 or PDMA2	-	PSDOUT0 7,8 (Surr. L/R)
PDMAi 7,8 or PDMA3	-	PSDOUT0 10,11(AC'97 S/PDIF)

Table 4-3. DMA to I²S / AC-Link Time Slot Mapping

For more information on the AC-link time slot definition, codec IDing, AMAP and similar topics, please, refer to the industry standard AC'97 specification Rev 2.2.

MT10: Interleaved Playback DMA Current / Base Address

Index: 10h - 13h

Default Value: 00000000h. PDMAi interleaves 8 outbound data slots, each with 32-bit from the system memory to physical outputs.

Bit	Attribute	Description
31:2	R/W	Write the Playback DMA base address in dword units Read current address in dword units.
1:0	R00b	- (This DMA channel supports dword boundary only)

MT14: Interleaved Playback DMA Current / Base Count

Index: 14h - 16h

Default Value: 0000h

Bit	Attribute	Description
18:0	R/W	Write the Interleaved Playback DMA initial buffer size in dword units minus one. This register auto-decrements as the DMA transfer progresses. It reinitializes automatically to the original buffer size once it reaches 0 count. Read the current Playback DMA pointer.

MT18: Global Playback and Record DMA Start / Stop

Index: 18h

Default Value: 00h.

Software should always resort to RMW (read modifiy write) to guarantee unintended interference with other channels that may be simultaneously active.

Bit	Attribute	Description
7	R/W	1: SPDIFout/PDMA4 start; 0: SPDIFout/PDMA4 stop
6	R/W	1: PDMA3 start; 0: PDMA3 stop. Valid only when MT19>00b
5	R/W	1: PDMA2 start; 0: PDMA2 stop. Valid only when MT19>01b
4	R/W	1: PDMA1 start; 0: PDMA1 stop. Valid only when MT19=11b
3	R0	-
2	R/W	1: RDMA1 start; 0: RDMA1 stop
1	R/W	1: RDMA0 start; 0: RDMA0 stop
0	R/W	1: PDMAi/PDMA0 start; 0: PDMAi/PDMA0 stop

MT19: Interleaved Playback DMA Active Streams / PCI Burst Size

Index: 19h

Default Value: 00h.

Bit	Attribute	Description
7:2	R0	Reserved
1:0	R/W	00 (default): Burst all 8chs.*4=32 data slots interleaved on PDMAi 01: Burst first 6chs.*4=24 data slots on PDMAi. 10: Burst first 4chs*4=16. data slots on PDMAi. 11: Burst only first stereo pair, i.e. PDMA0 as 8 data slots. This is the mode for having 1 independent pairs, each with its own request/grant mechanism.

MT1A: Global Playback and Record DMA FIFO Underrun / Overrun

Index: 1Ah

Default Value: 00h.

This register alerts software of a DMA underrun/overrun condition by raising a "1" flag. Any flag triggers an interrupt. The status can be checked by reading

Bit	Attribute	Description
7	R/W/C	1: SPDIFout/PDMA4 underrun; 0: SPDIFout/PDMA4 normal. Write a 1 to clear.
6	R/W/C	1: PDMA3 underrun; 0: PDMA3 normal. Valid only when MT19>00b. Write a 1 to clear.
5	R/W/C	1: PDMA2 underrun; 0: PDMA2 normal. Valid only when MT19>01b. Write a 1 to clear.
4	R/W/C	1: PDMA1 underrun; 0: PDMA1 normal. Valid only when MT19=11b. Write a 1 to clear.
3	R0	-
2	R/W/C	1: RDMA1 overrun; 0: RDMA1 normal. Write a 1 to clear.
1	R/W/C	1: RDMA0 overrun; 0: RDMA0 normal. Write a 1 to clear.
0	R/W/C	1: PDMAi/PDMA0 underrun; 0: PDMAi/PDMA0 normal. Write a 1 to clear.

MT1B: Global Playback and Record DMA Pause / Resume

Index: 1Bh

Default Value: 00h.

Software should always resort to RMW (read modifiy write) to guarantee unintended interference with other channels that may be simultaneously active.

Bit	Attribute	Description
7	R/W	1: SPDIFout/PDMA4 pause; 0: SPDIFout/PDMA4 resume
6	R/W	1: PDMA3 pause; 0: PDMA3 resume. Valid only when MT19>00b
5	R/W	1: PDMA2 pause; 0: PDMA2 resume. Valid only when MT19>01b
4	-	1: PDMA1 pause; 0: PDMA1 resume. Valid only when MT19=11b
3	R0	-
2	R/W	1: RDMA1 pause; 0: RDMA1 resume
1	R/W	1: RDMA0 pause; 0: RDMA0 resume
0	R/W	1: PDMAi/PDMA0 pause; 0: PDMAi/PDMA0 resume

MT1C: Interleaved Playback DMACurrent/Base Terminal Count

Index: 1C - 1Dh

Default Value: 0000h

Bit	Attribute	Description
18:0	WO	Write the terminal count. This register also auto-decrements as the DMA transfer progresses. When it reaches 0, it generates and interrupt. Program the desired count in dword units minus one to determine the interrupt frequency desired.

4.2.3 Record DMA Stereo Pairs Registers

MT20: Record DMA 0 Current / Base Address

Index: 20h - 23h

Default Value: 00000000h. RDMA0 interleaves 2 slots, each with 32-bit data to the system memory.

Bit	Attribute	Description
31:2	R/W	Write the Playback DMA base address in dword units Read current address in dword units.
1:0	R00b	- (This DMA channel supports dword boundary only)

MT24: Record DMA 0 Current / Base Count

Index: 24 - 25h

Default Value: 0000h

Bit	Attribute	Description
15:0	R/W	Write the Record DMA 0 initial buffer size in dword units minus one. This register auto-decrements as the DMA transfer progresses. It reinitializes automatically to the original buffer size once it reaches 0 count. Read the current Record DMA pointer after having allowed at least 2 sample frames.

MT26: Record DMA 0 Current / Base Terminal Count

Index: 26h - 27h

Default Value: 0000h

Bit	Attribute	Description
15:0	WO	Write the terminal count. This register also auto-decrements as the DMA transfer progresses. When it reaches 0, it generates and interrupt. Program the desired count in dword units minus one to determine the interrupt frequency desired.

MT30: Record DMA 1 Current / Base Address

Index: 30h - 33h

Default Value: 00000000h. RDMA1 stereo, each with 32-bit to the system memory from physical inputs of PSDOUT1 in I²S form. Typically S/PDIF in but nothing precludes it from being an ADC data.

Bit	Attribute	Description
31:2	R/W	Write the stereo pair 1 Record DMA base address in dword units Read current address in dword units.
1:0	R00b	- (This DMA channel supports dword boundary only)

MT34: Record DMA 1 Current / Base Count

Index: 34h - 35h

Default Value: 0000h

Bit	Attribute	Description
15:0	R/W	Write the stereo pair 1 Record DMA initial buffer size in dword units minus one. This register auto-decrements as the DMA transfer progresses. It reinitializes automatically to the original buffer size once it reaches 0 count. Read the current Playback DMA pointer.

MT36: Record DMA1 Current / Base Terminal Count

Index: 36 - 37h

Default Value: 0000h

Bit	Attribute	Description
15:0	WO	Write the terminal count. This register also auto-decrements as the DMA transfer progresses. When it reaches 0, it generates and interrupt. Program the desired count in dword units minus one to determine the interrupt frequency desired.

4.2.4 Digital Loopback

The Envy24PT provides an extensive routing capability of the data streams, avoiding host loading if data transfer across the bus is not requested by the user. The routing is possible only in the I²S mode, i.e. CCS05[7]=1. Since the xDMAx may not be mapped into AC-link time slots consecutively, the digital loopback is not available when CCS05[7]=0. The following registers control the routing from numerous sources to various destination. Insertion of the stream routing functionality adds a maximum of a single sample cycle delay with respect to the original data. The switch matrix being so complex, careful register setting is crucial to avoid undesirable effects. For simplicity of the register description only pin names are used. Refer to the pin list for pin numbers and location.

The diagram below is a visual representation of possible connection. If a dot is missing on an intersection, it reflects the lack of routing capabitlity. The output DMA can only be routed to its intended physical output. However, any input can be looped back to any of the output. This is useful for digitizing an analog source and outputting on S/PDIF Out or the reverse, taking an S/PDIF input PCM stream and converting it to analog directly on the fly, swapping Left/Right channels, routing signals to different output pairs.

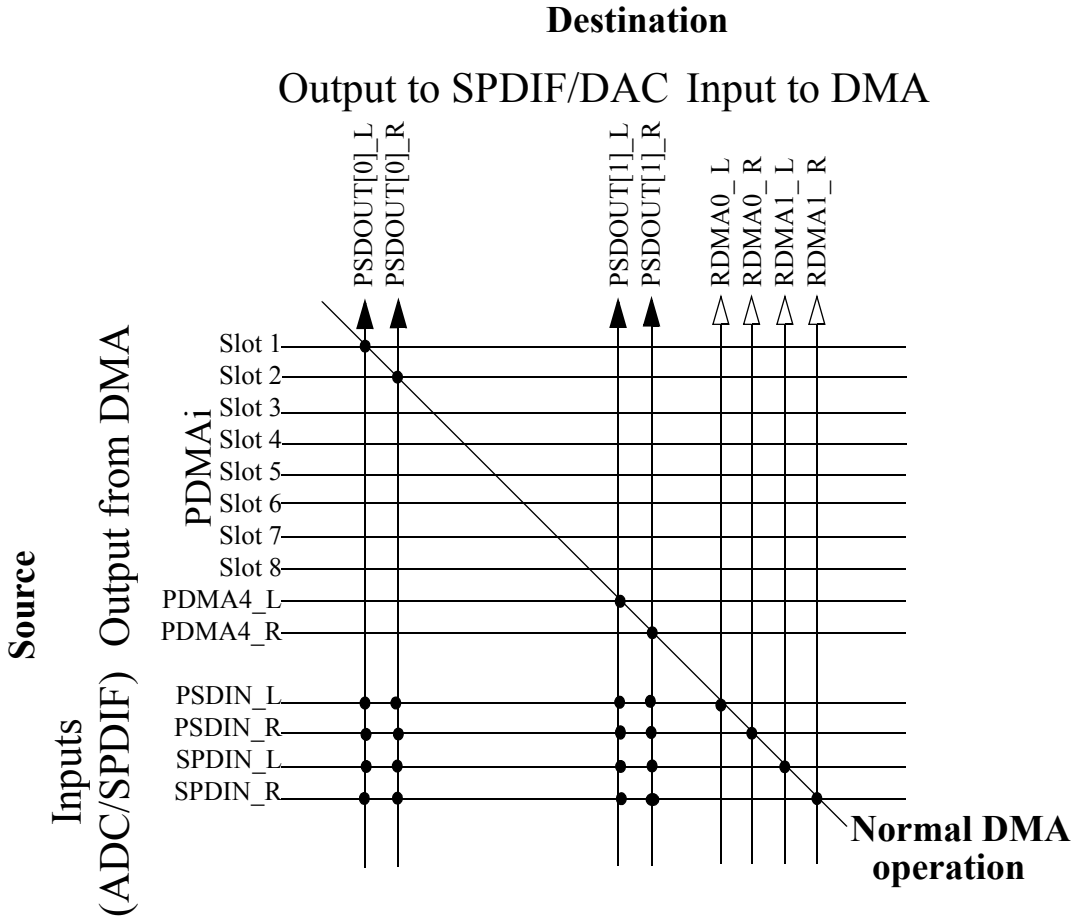


Figure 4-6. Data Stream Routing Capabilities

MT2C: Routing Control for Data to PSDOUT[0] and PSDOUT[1]

Default Value: 00h

Bit	Attribute	Description
31:11	-	Reserved
10:8	R/W	PSDOUT[0] Left source 000: from PDMAi slot 1 010: from PSDIN0 Left input loopback 011: from PSDIN0 Right input loopback 110: from SPDIN Left input loopback 111: from SPDIN Right input loopback Others: Reserved
7:6	R/W	Reserved
5:3	R/W	PSDOUT[1] Right source 000: from PDMA4 Right (2nd) slot 010: from PSDIN0 Left input loopback 011: from PSDIN0 Right input loopback 110: from SPDIN Left input loopback 111: from SPDIN Right input loopback Others: Reserved
2:0	R/W	PSDOUT[1] Left source 000: from PDMA4 Left (1st) slot 010: from PSDIN0 Left input loopback 011: from PSDIN0 Right input loopback 110: from SPDIN Left input loopback 111: from SPDIN Right input loopback Others: Reserved

4.2.5 Integrated S/PDIF Transmitter Register

MT3C: S/PDIF IEC958 Transmitter Control

Address Offset: 3Ch - 3Dh

Default Value: x000h

Description: This read/write register controls the S/PDIF functionality when bit CCS07[0] reports that S/PDIF is implemented. It will return 0000h when SPDTX, pin 92 left floating or pulled high. If S/PDIF is implemented for the final product, it will read 2000h at power-up. The register manages the bit fields propagated as channel status (or subframe in the V case). With the exception of V, this register should only be written when the S/PDIF transmitter is disabled (S/PDIF Enable/Disable bit CCS07[7] = 0). This ensures that control and status information start up correctly at the beginning of S/PDIF transmission.

Bit	Attribute	Description
15	R/W	Validity: This bit affects the "Validity flag", bit 28 transmitted in each subframe and enables the S/PDIF transmitter to maintain connection during error or mute conditions. 1: Tags both samples as invalid by setting bit 28, "Validity flag" to "1" 0: If a valid Left/Right pair was transmitted through S/PDIF, the Validity bit should be reset.
14 : 12	R/W	These bits declare the S/PDIF transmitter clock rate (64*fs) in the Channel Status Byte 3, low nibble if Consumer mode (MT3C[0] = 0) and Byte 0 (bits 7-6) and Byte 4 (bits 6-3) if Professional mode (MT3C[0] = 1). It will be set automatically by MT01 low nibble if master. In slave mode (MT01[4] = 1), to display the correct sampling rate, it must be written to reflect the external clock recovered. 000: 44.1 KHz 001: Reserved 010: 48 KHz (default) 011: 32 KHz 100: 88.2 KHz 101: 96 KHz 11x: Reserved
11	RW	Generation Level: Programmed according to IEC standards.
10:4	RW	Category Code. Programmed according to IEC standards.
3	R/Wh	Preemphasis. "1" : Indicates filter preemphasis is 50/15µs. "0" : Default is no Preemphasis.
2	R/W	Copyright "1" : Indicates copyright is not asserted. "0" : Copyright is asserted (default).
1	R/W	/PCM: Non-Audio Samples "1" : Set this bit for transmitting non-PCM audio samples such as AC-3. "0" : Indicates samples are linear PCM suitable for direct conversion to audio playback.
0	R/W	Professional "1" : Set Professional mode. Set this bit in conjunction with /PCM bit (above) for AC-3. "0" : Indicates Consumer mode (default).

4.2.6 VU Peak Meter Registers

MT3E: Peak Meter Index

Address Offset: 3Eh

Default Value: 00h

Bits	Attribute	Description
7:5	R000b	-
4:0	R/W	Peak meter stream index 00000: Playback stream 1 (PDMAi slot 1) 00001: Playback stream 2 (PDMAi slot 2) 00010: Playback stream 3 (PDMAi slot 3) 00011: Playback stream 4 (PDMAi slot 4) 00100: Playback stream 5 (PDMAi slot 5) 00101: Playback stream 6 (PDMAi slot 6) 00110: Playback stream 7 (PDMAi slot 7) 00111: Playback stream 8 (PDMAi slot 8) 01000: S/PDIF Left stream (PDMA4 slot 1) 01001: S/PDIF Right stream (PDMA4 slot 2) 01010: Record0 Left stream (RDMA0 slot 1) 01011: Record0 Right stream (RDMA0 slot 2) 01100: ignored. 01101: ignored. 01110: ignored. 01111: ignored. 10000: ignored. 10001: ignored. 10010: Record1 Left stream (RDMA1 slot 1, typ. S/PDIF Right input stream) 10011: Record1 Right stream (RDMA1 slot 2, typ. S/PDIF Right input stream) 10100: ignored. 10101: ignored. others: ignored.

MT3F: Peak Meter Data

Address Offset: 3Fh

Default Value: 00h

Bits	Attribute	Description
7:0	R	Peak data derived from the absolute value of 9 msb. 00h min - FFh max volume. Reading the register resets the meter to 00h.

4.2.7 Concurrent Stereo Pairs Playback DMA Registers

The following figure is a visual representation of the stereo pairs data transfer mechanism. This is an alternative to the default interleaved DMA method. In this mode the data is not packed tightly for time correlation. It allows independent stereo pair operation. A 12 layers deep buffer structure is implemented for a seamless flow of each stream. If the PDMAi burst size is left at 8, no stereo pair DMA is available except for SPDIFout/PDMA4 and Record DMAs which are always independently controllable. As the burst size of PDMAi is decreased by writing to MT19, independently controllable playback stereo pair DMAs become available. 32-bit data transfers are used regardless of the audio data resolution. All transfer data are left (MSB) justified. Each transfer request results into a PCI bus master burst cycle. The burst size is always 8 PCI data cycles long, i.e. Left and Right for 4 consecutive sampling times. All stereo DMA pairs behave similarly.

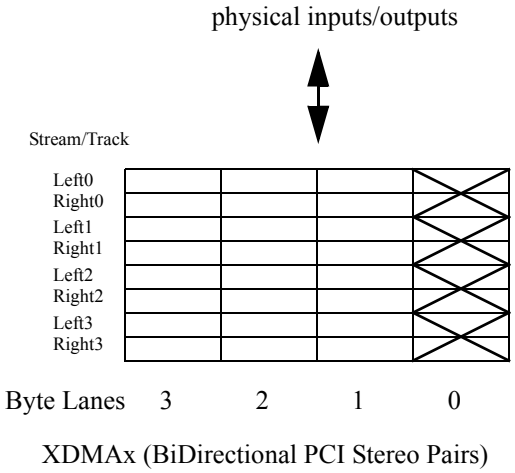


Figure 4-7. Stereo Pairs DMA Playback

MT40: SPDIFout / PDMA4 Playback DMA Current / Base Address

Index: 40h - 43h

Default Value: 00000000h. SPDIFout/PDMA4 stereo, each with 32-bit from the system memory to physical outputs of IEC958 line driver and a copy toPSDOUT4 in I²S form.

Bit	Attribute	Description
31:2	R/W	Write the Playback DMA base address in dword units Read current address in dword units.
1:0	R00b	- (This DMA channel supports dword boundary only)

MT44: SPDIFout / PDMA4 Playback DMA Current / Base Count

Index: 44h - 45h

Default Value: 0000h

Bit	Attribute	Description
15:0	R/W	Write the stereo pair 4/SPDIF out DMA initial buffer size in dword units minus one. This register auto-decrements as the DMA transfer progresses. It reinitializes automatically to the original buffer size once it reaches 0 count. Read the current Playback DMA pointer.

MT46: SPDIFout / PDMA4 Playback DMACurrent / Base Terminal Count

Index: 46 - 47h

Default Value: 0000h

Bit	Attribute	Description
15:0	WO	Write the terminal count. This register also auto-decrements as the DMA transfer progresses. When it reaches 0, it generates and interrupt. Program the desired count in dword units minus one to determine the interrupt frequency desired.

Electrical Specifications

5.1 Maximum Ratings

Table 5-1. Maximum Ratings

Parameter	Min	Typ	Max	Unit
Storage Temperature	–55		150	°C
Operating Ambient Temperature	0	25	70	°C
DC Supply Voltage (Analog and Digital)	3.0	3.3	4.0	V
I/O Pin Voltage	GND – 0.5		VCC	V
Power Dissipation			TBD	W

5.2 Electrical Specifications

Table 5-2. DC Characteristics

(TA=25°C, VCC = 3.3V ± 5%; GND = 0V; 50pF Load)

Symbol	Parameter	Min	Typ	Max	Unit
VIN	Input Voltage Range	–0.3		VDD+0.3	V
VIL	Input Low Voltage			0.3 x VDD	V
VIH	Input High Voltage	0.7 x VDD			V
VOL	Output Low Voltage			0.4	V
VOH	Output High Voltage	2.4			V
IIL	Input Leakage Current	–10		10	µA
VOL	Output Leakage Current	–10		10	µA
–	Output Buffer Drive Current		TBD		mA
–	S/PDIF Transmit Output Drive Current		6		mA

Table 5-3. Power Consumption

(TA=25°C, VCC = 3.3V ± 5%; GND = 0V; 50pF Load)

Symbol	Parameter	Min	Typ	Max	Unit
IVDD	Supply Current: Power Up		TBD		mA
IVDD	Supply Current: Partial Power Up		TBD		mA
IVDD	Supply Current: Partial Power Down		TBD		mA
IVDD	Supply Current: Power Down		TBD		mA

5.3 AC Timing Characteristics

(Test Conditions: TA=25°C, VCC = 3.3V ± 5%; GND = 0V; 50pF Load)

Table 5-4. Cold Reset

Symbol	Parameter	Min	Typ	Max	Unit
TRST_LOW	PRST# Active Low Pulse Width	1			µs
TRST2CLK	PRST# Inactive to PBCLK / SPSCLK Startup Delay	162.8			ns

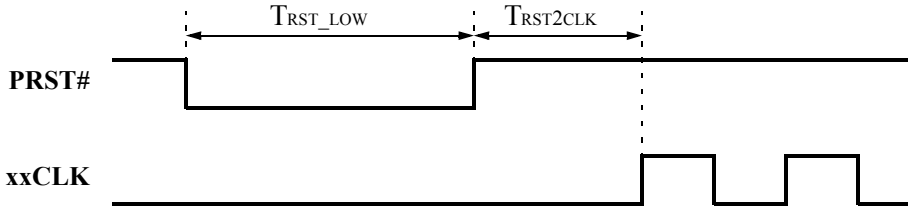


Figure 5-1. Cold Reset Timing

Table 5-5. Warm Reset

Symbol	Parameter	Min	Typ	Max	Unit
TSYNC_HIGH	PSYNC Active High Pulse Width		1.3		µs
TSYNC2CLK	PSYNC Inactive to PBCLK Startup Delay	162.8			ns

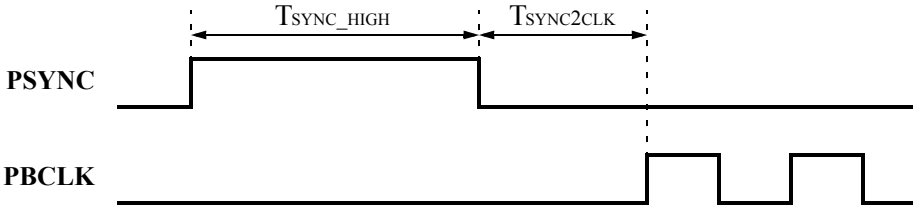


Figure 5-2. Warm Reset Timing

Table 5-6. Slave Mode Master Clock Delay

Symbol	Parameter	Min	Typ	Max	Unit
TSPI2MCK	SPMCLKIN to PMCLK Delay		4		ns
TSPI2SPO	SPMCLKIN to SPMCLKOUT Delay		5.5		ns

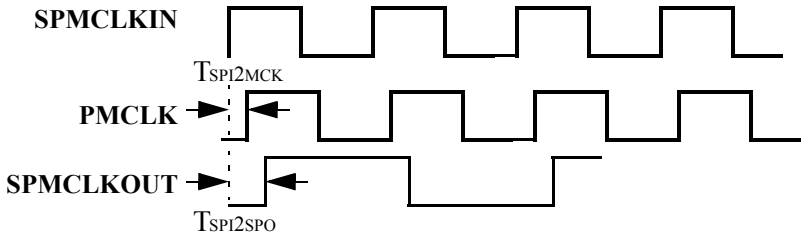


Figure 5-3. Master Clock Delay

Table 5-7. PBCLK / PSYNC Timing

Symbol	Parameter	Min	Typ	Max	Unit
	PBCLK Frequency				MHz
TCLK_PERIOD	PBCLK Period				ns
	PBCLK Output Jitter		TBD	750	ps
TCLK_HIGH	PBCLK Pulse Width (high)				ns
TCLK_LOW	PBCLK Pulse Width (low)				ns
TCLK_DC	PBCLK Duty Cycle				%
	PSYNC Frequency				KHz
TSYNC_PERIOD	PSYNC Period				µs
TSYNC_HIGH	PSYNC Pulse Width (high)				µs
TSYNC_LOW	PSYNC Pulse Width (low)				µs

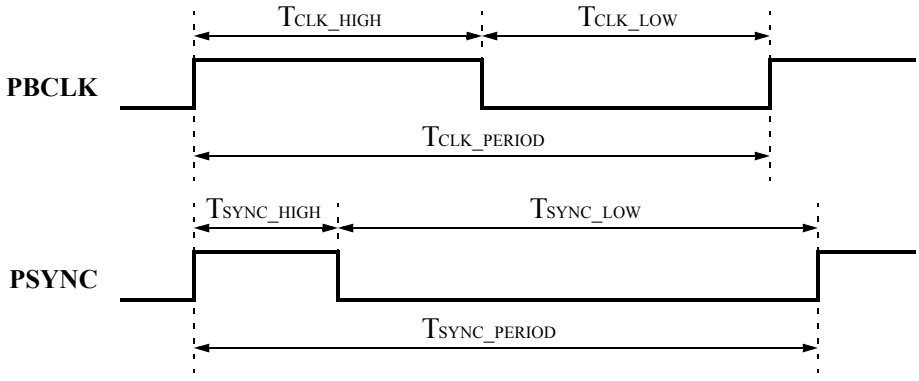


Figure 5-4. PBCLK to PSYNC Timing

Table 5-8. Setup and Hold

Symbol	Parameter	Min	Typ	Max	Unit
TSETUP1	SDOUT Setup to falling edge of PBCLK	15			ns
THOLD1	SDOUT Hold from falling edge of PBCLK	5			ns
TSETUP2	PSYNC Setup to rising edge of PBCLK	15			ns
THOLD2	PSYNC Hold to rising edge of PBCLK	5			ns

Note: SDATA_IN seup and hold calculations determined by AC'97 controller propagation delay.

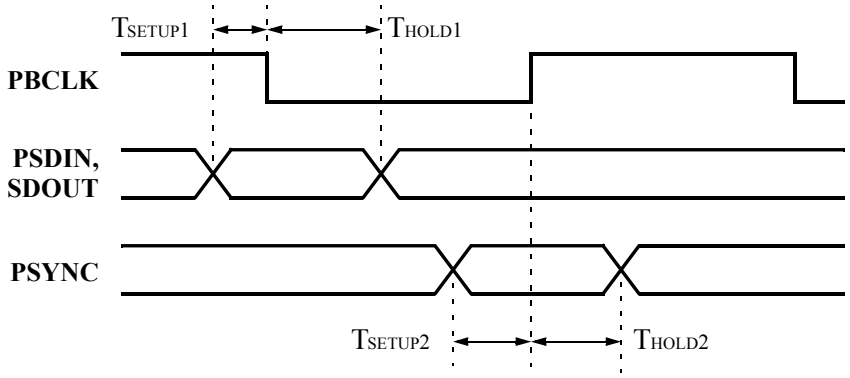


Figure 5-5. Setup and Hold Time

Table 5-9. Rise and Fall Time

Symbol	Parameter	Min	Typ	Max	Unit
TRISE	PBCLK Rise Time	2		6	ns
TFALL	PBCLK Fall Time	2		6	ns
TRISE	PSYNC Rise Time	2		6	ns
TFALL	PSYNC Fall Time	2		6	ns
TRISE	PSDIN Rise Time	2		6	ns
TFALL	PSDIN Fall Time	2		6	ns
TRISE	SDOUT Rise Time	2		6	ns
TFALL	SDOUT Fall Time	2		6	ns

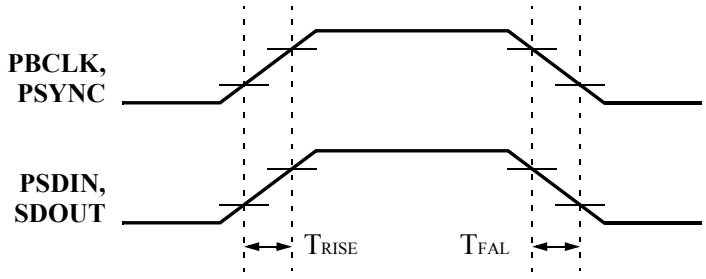


Figure 5-6. Rise Time and Fall Time

Table 5-10. AC-link Low Power Mode

Symbol	Parameter	Min	Typ	Max	Unit
T_{S2_PDOWN}	End of Slot 2 to PBCLK to PSDIN Low			1	µs

Note: CBCLK/PBCLK not to scale.

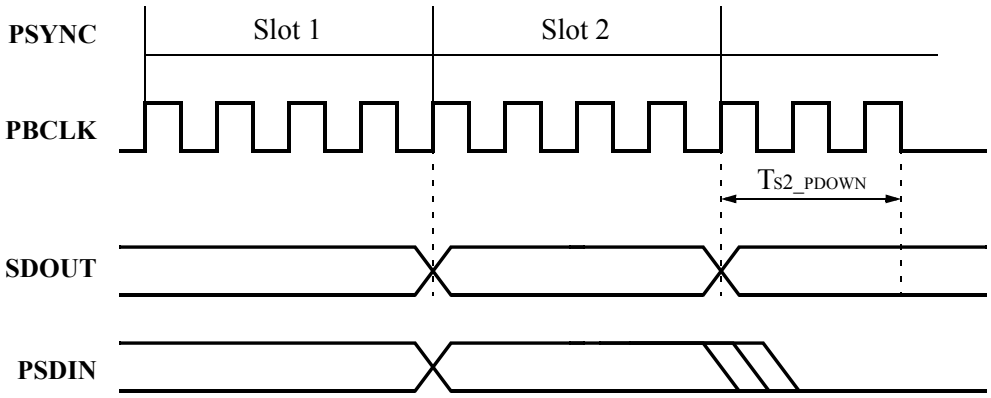


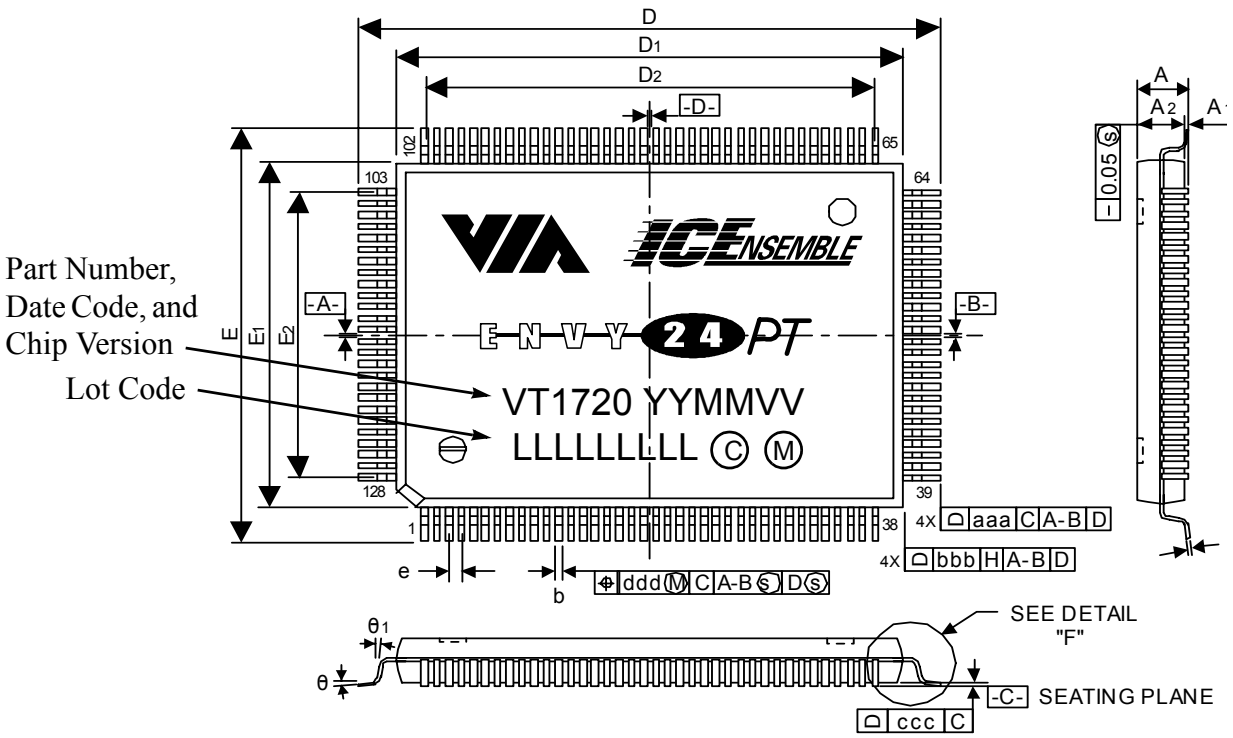
Figure 5-7. AC-Link Power Mode Timing

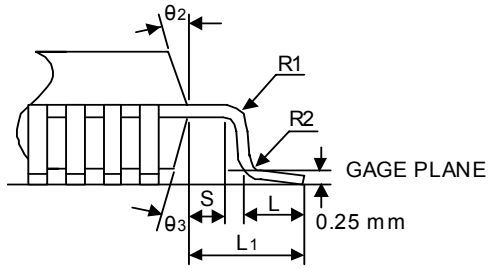
Mechanical Specifications

6.1 Thermal Specifications

Parameter	Min	Typ	Max	Unit
Thermal Resistenace θ_{JA} (Still Air)		TBD		°C/W
Junction Temperature		TBD		°C

6.2 Package Dimensions





DETAIL "F"

CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	3.40	—	—	0.134
A1	0.25	—	—	0.010	—	—
A2	2.50	2.72	2.90	0.098	0.107	0.114
D	23.20 BASIC			0.913 BASIC		
E	17.20 BASIC			0.677 BASIC		
D1	20.00 BASIC			0.787 BASIC		
E1	14.00 BASIC			0.551 BASIC		
D2	18.50 BASIC			0.728 BASIC		
E2	12.50 BASIC			0.492 BASIC		
R1	0.13	—	0.30	0.005	—	0.012
R2	0.13	—	—	0.005	—	—
θ	0	—	7	0	—	7
θ1	0	—	—	0	—	—
θ2	15 REF			15 REF		
θ3	15 REF			15 REF		
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L1	1.60 REF			0.063 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BASIC			0.020 BASIC		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

NOTES :

DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

Figure 6-1. 128-Pin PQFP Package Mechanical and Marking Specifications